REMARKS

In this Amendment, Applicant has amended Claims 8, 9, 21 – 24, and 26 – 27; and added new Claims 28 – 30 to overcome the rejections and further specify the embodiments of the present invention. It is respectfully submitted that no new matter has been introduced by the amended and new claims. All claims are now present for examination and favorable reconsideration is respectfully requested in view of the preceding amendments and the following comments.

PRIORITY:

Examiner indicates that a certified copy of foreign priority document has not been submitted. Applicant respectfully submits that a certified copy of foreign priority application will be submitted in due course.

INFORMATION DISCLOSURE STATEMENT:

The Information Disclosure Statement ("IDS") filed on June 26, 2006 has been resubmitted under 37 CFR 1.97(b)(4). Therefore, no fee is required. Proper recognition and consideration of the documents cited in the IDS is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 112 FIRST PARAGRAPH:

Claims 17 – 19 and 21 – 27 have been rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement.

It is respectfully submitted that in view of the amendments, the rejection has been overcome. Applicant respectfully submits that the embodiments of the present invention as in Claims 17 – 19 and 21 – 27 are enabled to a person of ordinary skill in the art. An input register is common to all embodiments of the invention and all claims. Such a register is shown as 12 in Fig. 5, and as 21 in Fig. 6. In Fig 6, the register is shown as consisting of D flip-flops, for example, 20. The register is also shown as 39 in Fig. 8.

Fig 12, about which the objection is raised, does not show the register, or in fact any other element such as the Monitoring Services and Control unit 17. Such items were considered by Applicant to have been sufficiently described in prior paragraphs so as not to require a repeated description. Fig 12 shows unconnected input lines, which given the detail presented earlier in the description, and is sufficient for one skilled in the art to properly understand how to implement the invention. In addition, the Logic Processing Circuits (LPC) are shown in Fig 8, Fig 9 and Fig 12 using identical graphic symbols with inputs labelled 1 ... N.

Figure 12 is described on page 25 line 23, "Figure 12 shows conceptually ...". It says explicitly "LPC 102 and 103 are fed in parallel, which is to say that all input signals are applied to them identically". Although the input register is not mentioned explicitly, the LPC input circuits described are never shown or described anywhere in the application as being fed from anything other than the input register. The clear implication of the specification is that the LPCs of Figure 12 are fed from an input register.

One skilled in the art will know that the purpose of such a register is to sample the signals applied to the inputs of the register, (the D pins on the D flip-flops), and to store the input values on the flip-flops for later use. Additionally, one skilled in the art will know that time must be allowed for the storage process to take place and for the stored value to propagate to the flip-flop outputs, and to settle. To use the value on the register output while it is transient and prior to settling would be to use a signal value that might be in error. A register cannot be used properly without ensuring proper management of setup, hold, and output settling times and so managing such aspects is a routine matter for one skilled in the art.

Regarding Claim 17, the intention of the phrase objected to by the Examiner was to claim an input register that sampled its inputs, stored the input value and provided the stored and settled value to the LPC, guaranteeing that the values applied to the two LPCs are identical when read by the LPCs. It is a normal function of a register as used in the art of electronic engineering to provide values that are 'settled and not transient when used'. The amended claim reads "said input register providing sampled and stored values

identically to each user control program circuit". The same points apply to Claim 18 – 19, although the amended claim also changes "valves" to "values", which is an obvious typographic error.

Regarding Claims 21 and 22, on page 7 line 33 of the specification, it says "In the invention, the programmable interconnections are used to interconnect the logic elements as required to implement the logic circuit representing the required user control program. Applicant will refer to the circuit as a Logic Processing Circuit (LPC). The user control program is provided to the Programmable Controller in the form of a bit pattern used to configure the switches." This makes it clear that the LPC is configured into the programmable logic hardware. Configuring programmable logic hardware is a routine matter.

Fig 9 shows an LPC 59 (also marked as LPC) containing flip-flops as at 60, and marked 1 ... 8, connected as at 63 to form a shift register. The flip-flops connected as a shift register represent the 'means of access'. The "configured means of access" are described from page 16 line 21 to page 17 line 32 of the specification as originally filed. The description explicitly states (page 17) that LPC 59 is "arranged to exchange data (that is 'read and write') with an external circuit 62" and that the flip-flops are "configured in the LPC". This explicitly supports claim 21.

Page 17 line 27 also says "To allow the LPC flip-flops 60 to function both as user circuit devices and as part of the endless loop shift register 61, support circuits are provided. Figure 10 shows such a support circuit." and there is a full description of the operation of the circuits. This explicitly describes using the flip-flops for the dual purpose claimed in claim 22.

Page 18 line 5 of the specification says "The application of the support circuit in Figure 10 around the flip-flop 66 imposes some restrictions on how the flip-flop may be used in the user control program circuit" emphasizes that the circuit in Figure 10 is used in the user control program.

The section *Built-in means of access* states that "A PLD may be provided with built-in circuits to support access during operation to state data stored in the user

accessible flip-flops it contains" and also "This invention can use such an arrangement for reading and writing state data as an alternative to the means previously discussed if convenient." This refers to the possibility of circuits built into the fabric of the FPGA by the FPGA manufacturer. The separate description of built in access circuits emphasizes the separate nature of the configured means described on page 17-18, and emphasizes that the inventor envisages both possibilities. Claim 21 specifically claims access configured in the user control program circuit.

Therefore, it is respectfully submitted that the original specification does sufficiently disclose the features of Claims 17 – 19 and 21 – 27, and a person of ordinary skill in the art is able to make and use the present invention as amended based on the disclosure of the specification.

Therefore, the rejection under 35 U.S.C. § 112, first paragraph has been overcome. Accordingly, withdrawal of the rejections under 35 U.S.C. § 112, first paragraph, is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 102:

Claims 3, 4, 8, 9, 17 – 19 and 21 – 27 have been rejected under 35 U.S.C. § 102 (e) as allegedly being anticipated by Vasko (US 6,463,339), hereinafter Vasko.

Applicant traverses the rejection and respectfully submits that the presently claimed invention is not anticipated by the cited reference. However, before the discussion of the differences between the claimed invention and Vasko, Applicant believes that it is necessary to clarify certain terms and interpretations related to the art of the present invention as follows.

Clarifications

The discussion regarding the claims should be considered in light of this Clarifications section.

"State Data" Definition

The term "State Data" as used in the specification refers to the kind of data that defines the state of a Finite State Machine (FSM).

Applicant will describe the operation of an FSM in a generalized way. In an FSM, a register contains a pattern of '0's and '1's indicative of the 'state' currently active in the FSM. The pattern persists for a finite amount of time until it is replaced by another state pattern indicating another state is active in the FSM. In general, inputs applied to the state machine direct the changing of states. The way state activity changes in response to the inputs is most commonly described on a state diagram. State changes depend both on which inputs are true and false, and on the state that is active when the inputs are interrogated. The state of the state machine is therefore a function of the past history of the inputs to the FSM, not the inputs as they are currently applied.

The state pattern is stored data and there must be a clock of some form to manage ordered sequencing of the state activity. Inputs are interrogated under the control of the clock and therefore state activity changes are timed by the clock. Active states therefore also last for a finite amount of time, the minimum possible being determined by the minimum interval between input interrogations.

More generally, any single-clock-domain synchronous digital circuit containing storage elements such as flip-flops is a state machine, although many such circuits will be too complex to describe on a state diagram and will be best understood by subdivision into smaller individually comprehensible sub-systems. This description applies to counters, microprocessors, memories, and complete computers. At any point in time the pattern of '1's and '0's in the storage elements of such a circuit defines the circuit state, and therefore how it will react to whatever input values are applied when the circuit inputs are next interrogated.

As described in the specification, the circuit is a synchronous logic circuit having registered inputs, internal flip-flops and timed by a clock. The state data referred to in the claims is the data stored in the flip-flops from one clock edge to the next.

It should be noted that the description at page 10 line 17 says "The outputs 24 from the input registers are passed to the LPC [Logic Processing Circuit] 25, and are used by the user control program logic in the LPC together with internally stored state data to generate LPC outputs 26" and claim 3 refers to "a plurality of state data storage units storing the user circuit state data". The word "**the**" indicates that all of the state data is stored in the plurality of state data storage units. The data stored in the input register also falls within the broad definition of state data, although not state data internal to the LPC.

Applicant explicitly define the term "State Data" on page 11 at line 16 of the specification where it states:

> "State data is data stored internally within a circuit from one cycle of operation of the circuit to the next where the circuit is such that the outputs from clock pulse to clock pulse depend on the values stored as well as the inputs to the circuit. State data may be as simple as a bit stored on a flip-flop as at 34, or as complex as an array of records stored in a memory."

Clearly this definition implies both storage (e.g., flip-flops) and clocked operation.

General Discussion

It is respectfully submitted that Vasko does not refer to state data. Applicant suggests that this is consistent under Vasko's purpose and implementation and is not an oversight. The presence of state data is a reliability issue because the state data is stored in flip-flops, and Vasko is aiming at a very reliable controller. An electro-magnetic disturbance originating from nearby electrical circuits, a spark, lightning or a cosmic particle can invert the state of a flip-flop causing circuit malfunction. In particular, the rate of disruption by cosmic particles is altitude dependent making this source a greater issue in aviation applications. The sensitivity to such disruptions is also dependent on gate array feature size, which may have been the reason why Vasko nominates 'low complexity' FPGAs (See Abstract). Even though Vasko's circuits are proposed in order to detect such errors, reducing the errors themselves is an advantage in a high reliability system.

Any digital circuit without state data can only consist of purely combinational logic and therefore the voltage levels in the circuit that may have been disturbed by a

(non-destructive) electro-magnetic pulse will rapidly return to levels defined purely by the input signals once the disturbance is over. This would support Vasko's choice to implement purely combinational logic, and such a system would be well suited to safety interlocking systems, such as the light fences quoted by Vasko, column 2 line 38, and similar applications. If state data is present the circuit is more vulnerable.

For any particular controller application, sufficient reliability depends on the controller error rate, and the rate of errors that can be accommodated by the process under control. Clearly, a controller for a lighting system can live with a higher error rate, say one failure once per ten or 100 years, than a controller for a nuclear reactor.

In fact, Vasko does not appear to have considered any specific method of implementing his control program, other than that Vasko's claims refer to FPGA outputs that are "Boolean functions of the gate array inputs" and as described with reference to Figs 5 and 6. Applicant considers that Applicant's FPGA outputs, or those of any circuit containing state data, cannot be written as a boolean expression in terms only of the inputs. Instead the FPGA outputs are functions of the state data of the circuit configured into the FPGA, as well as possibly, but not necessarily the FPGA inputs.

Vasko has not addressed any of the issues of implementing a control program circuit including state date storage in a way that provides functionality, monitoring and control as would be expected in a normal programmable controller.

Disclosure

FPGAs resemble an engineer's component cabinet in that they contain many different types of digital components that can be chosen and used in a design, or not, as the engineer requires. Where the components in the cabinet require physically interconnecting, the FPGA components are electrically interconnected via the configuration process. The raison d'etre for an FPGA is to avoid, at least in part, the component cabinet and the physical wiring.

FPGAs can include date storage (flip flops) and Vasko describes using an FPGA. But Vasko does not describe a circuit employing data storage or flip flops.

An applicant cannot say "I am going to include a component in my claim because I had one in my cabinet, even though I did not use it in my circuit or disclose it in my description". For the same reason, the Examiner cannot say that Vasko discloses the use of a component if the component simply exists unused in the otherwise-employed FPGA, and is not used in the circuit described in the specification.

Flip-flops, and Registers

A reading of the complete Vasko specification reveals that there is no mention of the use in Vasko's control program circuit of flip-flops or registers (arrays or sets of flip-flops). Vasko refers to all kinds of combinational logic elements, but never to any storage elements.

Vasko refers to memory cells that exist in the gate-array for the purpose of configuring the user circuit. These memory cells are not part of the operative user circuit and they only function to define how it is 'wired'. The contents of these memory cells is written when configuration is performed, and does not change until the user circuit is configured again.

Vasko does not disclose the use of flip-flops, or registers in the control program circuit.

Input Register

On the Examiner's assertion that Vasko discloses an Input Register in Fig. 2 for example (I/O blocks 40)- Vasko says "FIG. 2 is a block diagram of an example commercially available programmable gate-array showing component configurable logic blocks and input output blocks flexibly interconnected by a switch matrix controlled by programmable memory cells". In other words he is showing commercially available prior art.

The I/O Blocks 40 may in fact contain flip-flops or registers, or not depending on the specific gate-array chosen. Such registers, if they exist have the same status as the components in the engineer's components cabinet previously discussed, and their existence does not imply they are used. Vasko does not state that registers exist in the

I/O Blocks, nor does he describe any use at all of any flip-flops or registers in his specification.

Therefore, Vasko does not disclose the use of an input register.

Clocking Means

On the Examiner's assertion that Vasko discloses a clocking means in col. 6 lines 38-52, what Vasko says is "Such FPGAs 12 and 14 differ from microprocessors in that they do not sequentially decode instructions according to a clock to read and write from memory but instead are more accurately described as hardware interconnected logical gates that differ from wired together discrete logical gates only by the fact that the interconnections are affected by a reprogrammable set of memory cells 36."

In other words, Vasko says microprocessors use a clock, and also says that FPGAs are equivalent to electrically interconnected gates. Vasko does not associate a "clock" with the FPGA or say that an FPGA has a clock. The use of an FPGA does not imply the use of clocked logic, i.e., synchronous logic.

Therefore, Vasko does not disclose the use of a clock.

State Data

The Examiner asserts that Vasko discloses user circuit state data in at least col. 3 line 56 - col. 4 line 2, col. 7 lines 15-30, col. 8 lines 51-61, and col. 13 lines 6-10. Applicant argues as follows.

All the references quoted refer to states of logic levels, signal levels or output levels. The word 'state' has multiple meanings. Applicant uses the term "State Data" has the meaning as discussed above, and as defined at the top of the section of the specification headed "State data and implications."

Vasko does not refer to or disclose the use or existence of State Data as defined or any kind of data stored in the circuit configured into the FPGA.

State Data Storage Units

Vasko does not refer to or disclose the use or existence of State Data. It follows that Vasko does not refer to or disclose state data storage units.

Means of Access

Vasko does not refer to or disclose the use or existence of state data storage units. It follows that Vasko does not refer to or disclose a means of access to the values stored in state data storage units.

Regarding the Examiner's response in paragraph 10 of the Office Action, Claim 3 depends on three important elements, which are:

- an input register,
- state data storage units, and
- a means of access for the monitoring system to the state data storage units.

These elements are considered useful for proper management of access to the state data in the control program circuit. The applicant's previous remark was directed to elements that Vasko did not disclose, rather than to the detail of what Vasko did disclose, and the applicant argues that Vasko does not disclose any of these three elements.

Arguments are presented for this assertion and all others below related to point 11 of Examiner's report under the earlier headings:

- Clarifications - State Data Definition
- Clarifications - Flip-flops, and Registers
- Clarifications - Input Register
- Clarifications - Clocking Means
- Clarifications - State Data,
- Clarifications - State Data Storage Units
- Clarifications - Means of Access

The Applicant's arguments cited by the examiner were to further support the assertion that Vasko does not disclose any input register or other state data storage means. The presence of "flip-flops, sampling and storing values, or more complex

functions", "running, pausing and stopping", "settled signals", "clocked synchronous operation" could have implied or indicated the use of input registers or state data storage. For example, it might be possible to argue that storage means are implied by the disclosure of a clock. A circuit timed by a clock can be started - that is made to run - by enabling the clock; single stepped by issuing either a single clock pulse or a defined plurality of clock pulses if a single functional step requires a plurality of pulses; and paused or stopped by disabling the clock. The circuit state will be constant while the clock is disabled, and can only progress to successor states if the clock is enabled.

The features referred to by the Applicant in the previous response are all characteristic of systems that include state data, and therefore state data storage units (because state data is data stored from clock to clock). The fact that Vasko does not disclose them supports applicant's argument that Vasko does not disclose state data storage. A user circuit including State data storage is recited in claim 3.

With regard to claim 4, Vasko does not disclose the use of a clock in his implementation, and therefore it cannot be assumed that a clock is used.

Vasko does not disclose State Data as defined in the specification or input registers, and the arguments to that effect are as discussed in the sections "Clarifications – State Data"; and "Clarifications – Input Registers" above.

Vasko does not disclose the use of any clock, flip-flop or register, whether input register or internal state data storage unit, nor does Vasko disclose the use or existence of State Data as the term is defined in the specification.

Because Vasko does not disclose the use or existence of State Data or state data storage units, Vasko therefore also does not disclose a means of access to the values stored in state data storage units.

Claim 3

In Claim 3, Applicant claims:

- an input register for connection to process plant and/or machinery to provide sampled and stored input data in digital form,
- state data storage units storing the user circuit state data, and a means of access to said state data storage units,
- a monitoring device connected to the means of access,
- the means of access enabling the monitoring device to read/write the state data storage units.

Applicant asserts that Vasko's specification does not mention the use in Vasko's control program circuit of input, registers, state data, state date storage in his user circuit, or of a means of access to such stored data.

Arguments are presented for this submission under the earlier headings:

- Clarifications - State Data Definition
- Clarifications - Flip-flops, and Registers
- Clarifications - Disclosure - Input Register
- Clarifications - Clocking Means
- Clarifications - State Data,
- Clarifications - State Data Storage Units
- Clarifications - Means of Access

The Applicant respectfully submits that Claims 3 and 4 are allowable over Vasko.

Claim 17

According to David A. Rennels, (UCLA Computer Science), who is considered one of America's expert's on fault tolerance, "The SAPO computer built in Prague, Czechoslovakia was probably the first fault-tolerant computer. It was built in 1950–1954 under the supervision of A. Svoboda, using relays and a magnetic drum memory. The processor used triplication and voting (TMR)", (Triple Module Redundancy). The fact that TMR has been known for a long time is also illustrated by the example of a US patent, 4,375,683 FAULT TOLERANT COMPUTATIONAL SYSTEM AND VOTER CIRCUIT, H. Wensley, Mar. 1,1983, in which Figure 3 illustrates a TMR truth table.

Rennels also states "An approach called *design diversity* combines hardware and software fault-tolerance by implementing a fault-tolerant computer system using different hardware and software in redundant channels. Each channel is designed to provide the same function, and a method is provided to identify if one channel deviates unacceptably from the others". Both statements are made in an article written for the 1999 edition of the Encyclopaedia of Computer Science.

Vasko illustrates TMR in Fig. 1 and Design Diversity in his Figs 7 and 8, both with associated descriptions. The techniques used by Vasko are encompassed by TMR and Design Diversity. Clearly, the Examiner considered the combination of the control program as a circuit configured in an FPGA and fault tolerance techniques to be novel. The novelty in Vasko is presumably not due to the fact that he has combined the two well-known elements of a user circuit in an FPGA and fault-tolerance, both of which were well-known at the time. Applicant presumes that the Examiner considered it not obvious that such a combination can be made to work in a programmable controller product, nor is it obvious what form the combination should take. Applicant submits that it is further not obvious that it is possible to make the combination of Applicant's much more complex user program circuit and its functionality work together with fault-tolerance techniques, nor is it clear as to which of the many fault tolerance techniques available are most suited to use with the Applicant's complex circuit. Whereas Vasko's circuit as taught consists of purely combinational logic, Applicant's circuit has considerably more complexity in order to handle the exchange of state data between a monitoring system and a user circuit constructed around dual purpose multiplexed flip-flops (Fig. 10), fast user program swapping including the relocation of state data (Fig. 11), and to be capable of control functions such as starting, pausing, resuming and stopping (page 12 line 30) among others.

Applicant further submits that Claim 17 is not anticipated by Vasko as it is dependent on claim 4, which applicant submits is allowable, and for the further reasons stated above. The discussion above also applies to Claim 18 and 19. Claims 8, 9, 21 – 27 are dependant on at least Claim 4. Applicant submits that Claim 4 is allowable and Claims 8, 9, 21 – 27 are accordingly allowable as well.

Therefore, the newly presented claims are not anticipated by Vasko and the rejection under 35 U.S.C. § 102 (b) has been overcome. Accordingly, withdrawal of the rejection under 35 U.S.C. § 102 (b) is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 103:

Claims 15 – 16 have been rejected under 35 U.S.C. § 103 as allegedly being unpatentable over Vasko in view of Spiller (US 5,057,994), hereinafter Spiller.

Applicant traverses the rejection and respectfully submits that the embodiments of present-claimed invention are not obvious over Vasko in view of Spiller. As stated above, there are significant differences between the Vasko and the present invention. Therefore, there is no motivation or suggestion to combine Vasko and Spiller to achieve the present invention. Even if they are combined, a person of ordinary skill in the art will not discern the present invention at time of its invention.

Therefore, the newly presented claims are not obvious over Vasko in view of Spiller and the rejection under 35 U.S.C. § 103 has been overcome. Accordingly, withdrawal of the rejections under 35 U.S.C. § 103 is respectfully requested.

Having overcome all outstanding grounds of rejection, the application is now in condition for allowance, and prompt action toward that end is respectfully solicited.

Respectfully submitted,

JACOBSON HOLMAN PLLC

By_____
John C. Holman
Registration No. 22,769

Date: January 22, 2007
(202) 638-6666
400 Seventh Street, N.W.
Washington, D.C. 20004
Atty. Dkt. No.: P67300US0